

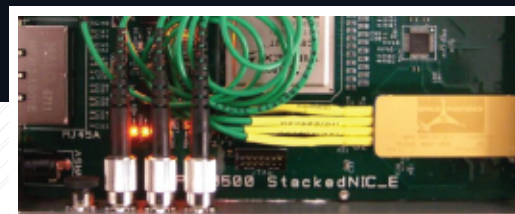


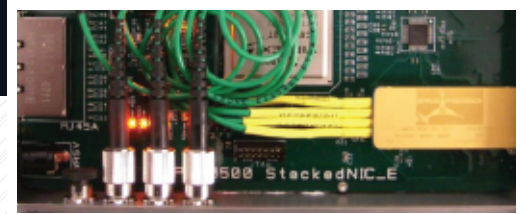
## FireRing®

### *HMP4-2500 StackedNIC\_E - User's Manual*

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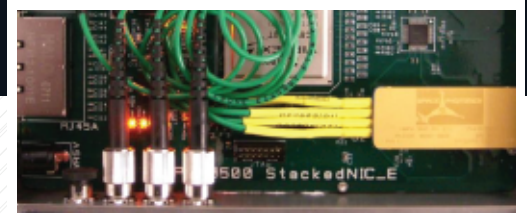
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## 1. Overview

The StackedNIC\_E board was developed for use in a multi-node 1393 FIRERING®. It is capable of transferring data at 2.5 Gbps using our fiber optic transceivers (HMP4-2500TX/HMP4-2500RX) or using optional coax mezzanine boards. Two Gigabit Ethernet Interfaces and one RS-232 port are provided for I/O. A set of differential SMA connections are provided for clock triggering and testing purposes. The board's functionality is controlled by programming the onboard Xilinx Virtex-5 FPGA.



## 2. Ratings

### 2.1 Power Supply Ratings

Parameter	Value
Absolute V in range	-0.3 V to 6 V
Operating V in range	3.81 V to 5.50 V
ESD rating, HBM	2kV
ESD rating, CDM	500V

Table 1 - Input Power Supply Ratings

### 2.2 HMP4-2500TX Optical Transmit Characteristics

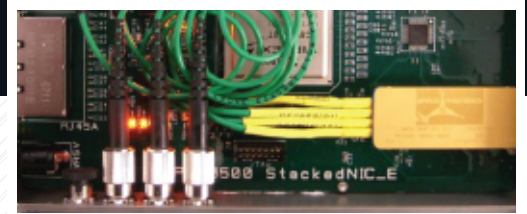
Parameter	Symbol	Min	Typical	Max	Units
Optical Output Wavelength	$\lambda_{out}$	1270	1310	1380	nm
Extinction Ratio	ER	--	-45	-40	dB
Optical Rise Time	$t_R$	0.6	1.5	3.0	ns
Optical Fall Time	$t_F$	0.6	1.5	3.0	ns
Duty Cycle Distortion	$t_{DCD}$	--	< 0.1	0.6	ns
Data Dependent Jitter	$d_{DJ}$	--	< 0.1	0.7	ns
Optical Output Power	$P_O$	-7.0	1.0	7.0	dBm

Table 2 - Optical Transmit Characteristics

### 2.3 HMP4-2500RX Optical Receive Characteristics

Parameter	Symbol	Min	Typical	Max	Units
Optical Wavelength	$\lambda_{in}$	1280	1310	1380	nm
Optical Sensitivity	$P_I$	-20	--	4	dB
Input Duty Cycle Distortion	$t_{DCD}$	--	--	1	ns
Input Data Dependent Jitter	$d_{DJ}$	--	--	0.76	ns
Signal Detect Assert Time	$t_{DCD}$	--	< 10	100	s
Signal Detect Deassert Time	$t_{DJ}$	--	< 10	350	s

Table 3 - Optical Receive Characteristics



## 3. Functional Description

### 3.1 Virtex-5 FPGA

A Xilinx Virtex-5 FPGA (XC5LX50T) and a configuration PROM (XCF32P) are installed on the StackedNIC\_E board.

### 3.2 I/O Interfaces

There are several I/O interfaces on the board. These are two Gigabit Ethernet ports, one RS-232 port, a differential set of SMA connections, the high speed fiber optic transceiver pair, and a set of 8 DIP switches and 4 LEDs connected to general purpose I/O pins on the FPGA.

#### 3.2.1 Gigabit Ethernet ports

Two Gigabit Ethernet ports are provided. Each of these ports connects to an Ethernet PHY chip (Broadcom BCM5461A1KFB). Each of these PHY chips is connected to the Virtex-5 FPGA, where MAC cores to interact with these PHY chips can be implemented, along with any higher level data processing functionality required. See Section 4.1 for pin connection information.

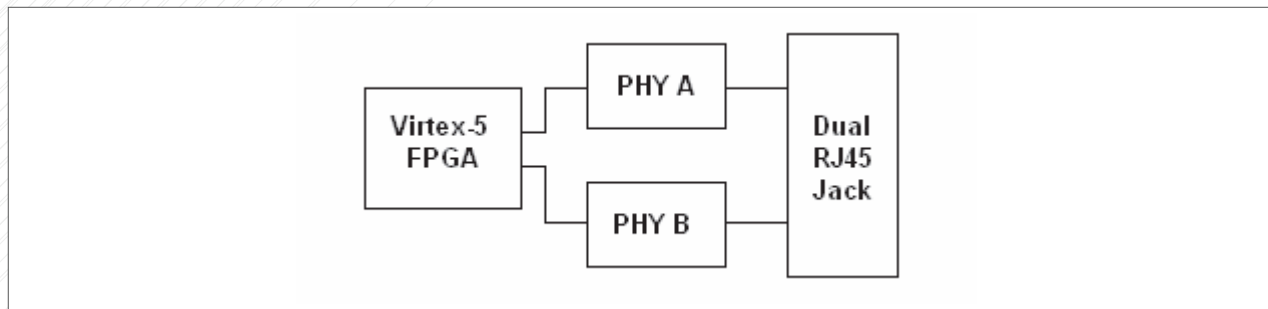


Figure 1 - Gigabit Ethernet Connection Overview

#### 3.2.2 RS-232 port

One RS-232 Port is provided for communication between the FPGA and a PC or other external device, using a standard, "straight-through" RS-232 cable. A MAX3223 is used as a level shifter. See Figure 2 for connection information. Hardware Flow Control is not provided. See Section 4.2 for pin connection information.

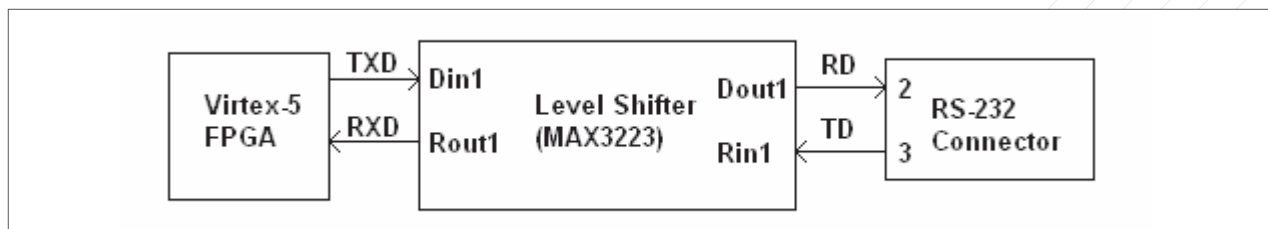
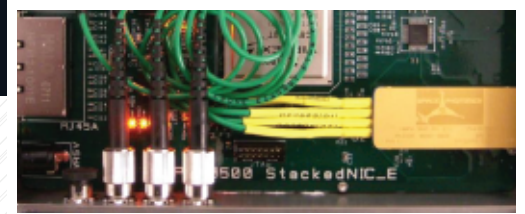


Figure 2 - RS232 Connections



### 3.2.3 SMA Connections

One differential pair of SMA connections to the FPGA is provided. On the FPGA, these are Global Clock Buffer pins, and, as such, may be used as inputs to the global clock tree of the FPGA, or they can be used for regular IO. They can be useful for debugging purposes to feed a clock to the FPGA or to output a clock to an oscilloscope for triggering. See Section 4.3 for pin connection information.

### 3.2.4 Transceivers

The Stacked NIC supports an HMP4-2500TX and HMP4-2500RX transceiver pair. The transmitter and receiver will support serial data transfer at up to 2.5 Gbps, and are connected to a RocketIO Multi-Gigabit Transceiver on the Xilinx Virtex-5 FPGA. The transmitter and receiver are currently available with 62.5/125um or 100/140um multimode fiber (call for other fiber requirements). Because 1393 requires 3 channels per card, only channels 1-3 on the transmitter and receiver are in use on this card. The HMP4-2500TX transmitter and HMP4-2500RX receiver are connected to one Virtex-5 RocketIO each, via a MAX3783 mux/demux chip. To use a given channel, the channel must be enabled via its enable line, and the MAX3783 must be configured accordingly. See Section 4.4 for pin connection and RocketIO details.

### 3.2.5 LEDs and Switched

LEDs and DIP switches connected to general purpose I/O pins on the FPGA are provided on the board. See Section 4.5 for pin connection details.

### 3.3 100 MHz Oscillators

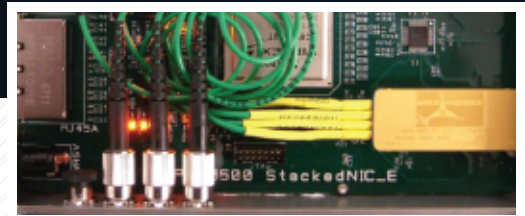
Two 100 MHz Oscillators, O1 and O2 are installed on the board and are connected to the Virtex-5 FPGA. O1 is connected to global clock pins on the FPGA, and may be used for general purposes. O2 is directly connected to the Virtex-5 RocketIO GCLKIN pins for the receive RocketIO. See Section 4.6 for pin connection details.

*NOTE: The transmit and receive RocketIOs are adjacent to each other on the FPGA die, so they may share reference clocks (GCLKIN).*

### 3.4 Cleanup PLL

A 100 MHz Cleanup PLL is included for cleaning up the clock recovered via the RocketIO receiver on the Virtex-5. For the 1393 protocol, it is necessary for the FBIUs (or BIUs in AS1393) to use the recovered clock from the receiver to clock the transmit data. The output of this cleanup PLL goes to the reference clock for the RocketIO. To implement the needed FBIU/BIU functionality, the recovered clock from the RocketIO receive block can be routed via the FPGA fabric to the input of the cleanup PLL.

The Cleanup PLL includes an Analog Devices ADF4001 chip, which must be programmed prior to use. Please see the ADF4001 datasheet for detailed information about this device. See Table 4 - Table 7 for ADF4001 settings. For use with Space.



Photonics FireRing® cores, we recommend the following settings in Table 4 - Table 7. A VHDL core is available for inclusion on the FPGA that will implement these. See Section 4.7 for pin connection information.

Bits	23:22	21	3	20:18	17:15	14:11	10	9	8	7	6:4	2	1:0
Values	00	0	0	011	111	0000	0	0	0	1	101	0	11

Table 4 - ADF4001 Initialization Latch Settings

Bits	23:22	21	3	20:18	17:15	14:11	10	9	8	7	6:4	2	1:0
Values	00	0	0	011	111	0000	0	0	0	1	101	0	10

Table 5 - ADF4001 Function Latch Settings

Bits	23:21	20	19:18	17:16	15:2	1:0
Values	000	0	00	00	0000000000000001	00

Table 6 - ADF4001 Reference Counter Latch Settings

Bits	23:22	21	20:8	7:2	1:0
Values	00	0	0000000000000001	000000	01

Table 7 - ADF4001 N (A,B) Counter Latch Settings

### 3.5 JTAG Configuration and Debugging Port

A JTAG port is provided for configuration and debugging purposes. Both the Xilinx Virtex-5 and the Xilinx XCF32P PROM can be programmed via this port. Board header H1 can be used to change the topology of the JTAG chain to include both the PROM and the FPGA, or to only include the FPGA. If pins 1 and 2 are shunted together and pins 3 and 4 are also shunted together, both the PROM and the FPGA will be included in the JTAG chain. However, by only shunting pins 2 and 3 together, the PROM is excluded, and only the FPGA will be in the JTAG chain.

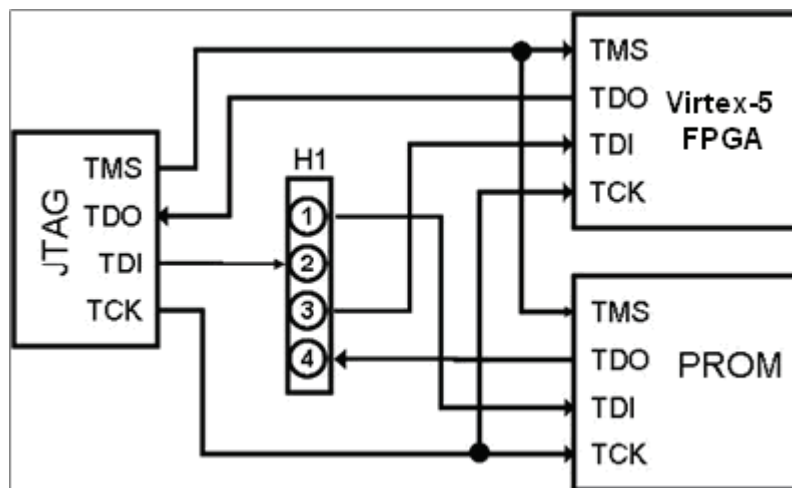
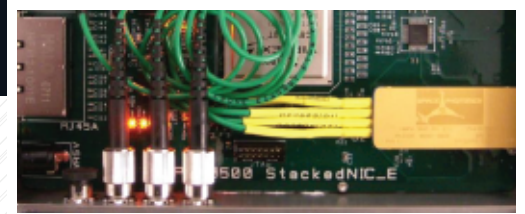


Figure 3 - JTAG Configuration Block Diagram



## 4. FPGA Pin-out Tables

### 4.1 Gigabit Ethernet PHY Connections

#### 4.1.1 Gigabit Ethernet PHY A

Virtex-5 pin	BCM5461 pin	Virtex-5 pin	BCM5461 pin	V	irtex-5 pin	BCM5461 pin
P34	CLK125	F34	TXD[2]		L33	RXD[7]
K34	MDIO	D34	TXD[1]		J32	RXD[6]
M33	MDC	E34	TXD[0]		G32	RXD[5]
H33	COL	F33	TXC		G33	RXD[4]
H34	CRS	E32	GTCLK		J34	RXD[3]
B32	TXD[7]	C34	TXEN		L34	RXD[2]
B33	TXD[6]	C32	TXER		M32	RXD[1]
C33	TXD[5]	N33	RXC		K32	RXD[0]
D32	TXD[4]	N34	RXER		K33	/RESET
E33	TXD[3]	N32	RXDV			

Table 8 – FPGA / PHY A pin Connections

#### 4.1.2 Gigabit Ethernet PHY B

Virtex-5 pin	BCM5461 pin	Virtex-5 pin	BCM5461 pin	V	irtex-5 pin	BCM5461 pin
AJ32	CLK125	AB32	TXD[2]		AF34	RXD[7]
AF33	MDIO	Y33	TXD[1]		AD34	RXD[6]
AH32	MDC	AA34	TXD[0]		AC32	RXD[5]
AC34	COL	AC33	TXC		AB33	RXD[4]
AD32	CRS	Y34	GTCLK		AE32	RXD[3]
V32	TXD[7]	W34	TXEN		AG32	RXD[2]
V33	TXD[6]	V34	TXER		AG33	RXD[1]
W32	TXD[5]	AH34	RXC		AE33	RXD[0]
Y32	TXD[4]	AJ34	RXER		AE34	/RESET
AA33	TXD[3]	AH33	RXDV			

Table 9 - FPGA / PHY B Connections

### 4.2 RS-232 Port

Virtex-5 pin	RS-232 function	RS-232 Connector Pin
AK33	TXD	2
AK34	RXD	3

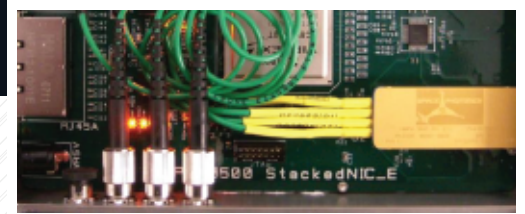
Table 10 - Virtex-5 / RS-232 Connections

### 4.3 SMA Connections

FPGA pins AH13 and AH14 connect to SMAs.

### 4.4 Transceiver Connections

To operate the 2.5 Gbps transceivers, the user must enable the desired transmit and receive channels, and must configure the Mux/Demux chip to route data between the Virtex-5 FPGA and the fiber optic transmitter and receiver.



## 4.4.1 Transceiver Enables

Table 11 shows the FPGA pin connections to the enable lines for the transmitter and receiver channel enable lines. All enable lines are active high.

TX/RX Channel Enable	Virtex-5 pin
TX Channel 1	AG5
TX Channel 2	AF5
TX Channel 3	AE6
RX Channel 1	J5
RX Channel 2	H5
RX Channel 3	G5

Table 11 - TX/RX Channel Enables

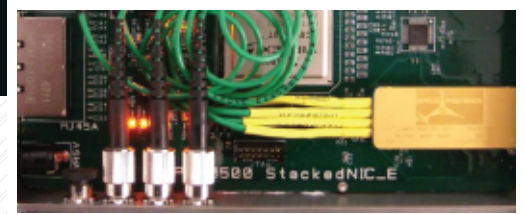
## 4.4.2 Mux/Demux Chip (MAX3783)

Table 12 shows the settings for the MAX3783 Mux/Demux chip. The Virtex-5 has builtin SERDES blocks, called RocketIOs. Two RocketIOs are used on this board, one for transmitting and one for receiving. The Mux/Demux chip is used to route serial receive data from the fiber optic receivers to the Virtex-5 RocketIO receiver, and also to route serial transmit data from the Virtex-5 RocketIO transmitter to the fiber optic transmitters. In the normal modes, data from the RocketIO transmitter is sent to all of the fiber optic transmitter channels, and the MAX3783 SELA and SELB pins are used to select which one of the fiber optic receiver channels will be connected to the Virtex-5 RocketIO receiver. In the loopback modes, which can be used for test purposes, data from a user selected fiber optic receiver channel can be routed through the Mux/Demux chip directly to a fiber optic transmitter channel.

	/LB 1A	/LB 2A	/LB 1B	/LB 2B	SELA	SELB
Normal modes						
Any TX, Ch1 RX	1	1	1	1	X	0
Any TX, Ch2 RX	1	1	1	1	1	1
Any TX, Ch3 RX	1	1	1	1	0	1
Loopback modes						
Send RX Ch2 signal to TX Ch1	0	X	X	X	X	X
Send RX Ch3 to TX Ch2	X	0	X	X	X	X
Send RX Ch2 signal to TX Ch1	1	X	0	X	1	X
Send RX Ch3 signal to TX Ch1	1	X	0	X	0	X
Send RX Ch2 signal to TX Ch2	X	1	0	X	1	X
Send RX Ch3 signal to TX Ch2	X	1	0	X	0	X
Send RX Ch1 signal to TX Ch3	X	X	X	0	X	X

Table 12 - Mux/Demux Chip Pin Settings

See Table 13 for FPGA pin connections to the Mux/Demux Chip.



Mux/Demux pin	/LB1A	/LB2A	/LB1B	/LB2B	SELA	SELB
FPGA pin	AB5	AA5	Y6	W6	M5	N5

Table 13 - Connections between FPGA and Mux/Demux Chip

## 4.4.3 Virtex-5 RocketIOs

To transmit serial data via the fiber optic transmitter, the transmitter in RocketIO transceiver 1 at site GTP\_DUAL\_X0Y2 on the Virtex-5 device is used.

To receive serial data via the fiber optic receiver, the receiver in RocketIO transceiver 1 at site GTP\_DUAL\_X0Y3 on the Virtex-5 device is used.

## 4.5 LEDs and Switches

### 4.5.1 LEDs

4 general purpose active-high LEDs are provided. See Table 14 for FPGA pin connection information.

LED name	LED13	LED14	LED15	LED16
FPGA pin	AK29	AK28	AK27	AK26

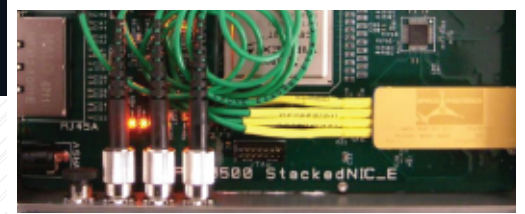
Table 14 - User LEDs and their FPGA connections

### 4.5.2 DIP Switches

A bank of 8 DIP switches is provided. Each of these switches is connected on one side to ground and on the other side to a Virtex-5 FPGA pin. The intent is that the user will utilize the PULLUP constraint on these pins in the Xilinx user constraint file (.ucf) so that this will implement active high switches. See Table 15 for pin connection information.

DIP switch number	FPGA pin
1	AH18
2	AG18
3	AH19
4	AH20
5	AG20
6	AG21
7	AH22
8	AG22

Table 15 - User DIP switches and their FPGA connections



## 4.6 100 MHz Oscillator Connections

Table 16 lists the FPGA pin connections to the 100 MHz oscillators on the board. Both of these are differential.

100 MHz Oscillator Pin	FPGA Pin
O1 (P,N)	AH15, AG15
O2 (P,N)	P4, P3

Table 16 - Clock Connections to the FPGA

## 4.7 Cleanup PLL Connections

Table 17 shows the control and status pins connected between the ADF4001 and the FPGA. These are used to configure the PLL for use. Table 18 shows the actual PLL input and output clock pin connections to the FPGA.

ADF4001 Pin	FPGA Pin
CLK	AK7
DATA	AK6
LE	AJ7
MUXOUT	AJ6

Table 17 - ADF4001 Connections to FPGA

PLL Clock Pin	FPGA Pin
PLL Input (P,N)	AL11, AL10
PLL output (P,N)	Y4, Y3

Table 18 - PLL Clock Pins